STRESSWORKSHOP CONFERENCE:

ABSTRACT:

Impact of Channel Stress in CFET Architectures

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Silicon MOSFET has continuously scaled since the advent of integrated circuit technology, providing our society ever increasing ability to manipulate data, store it, and communicate it. In order to sustain this scaling, technologists have had to implement novel transistors architectures such as FinFET in early 2010s and very recently gate-all-around (GAA) FET. While scaling also automatically resulted in significant performance gains during the 20th century, more recently the Silicon community has had to implement additional performance boosters – such as channel strain and high-K gate dielectrics.

This presentation focuses on CFET [1-4] which is universally recognized as next architecture revolution beyond GAA. CFET relies on technologies deployed by GAA architecture and extending them to enable stacking of PMOS on top of NMOS (or vice versa) in order to create significant density benefit without additional dimensional scaling. We will review state-of-the-art approach to CFET which includes monolithic stacking and cell-level intraconnects that are extension of BSPDN interconnects implemented in GAA technology. Lastly, we will discuss extending conventional strain approaches and simulated estimates of the channel stress and performance benefits [5] which will be crucial for the implementation of CFET in the future technology nodes.

[1] M. Radosavljević et al., "Demonstration of a Stacked CMOS Inverter at 60nm Gate Pitch with Power Via and Direct Backside Device Contacts," 2023 IEDM, pp. 1-4, doi: 10.1109/IEDM45741.2023.10413678.

[2] A. Vandooren et al., "Hybrid Channel monolithic-CFET with Si (110) pMOS and (100) nMOS," 2025 IEDM, pp. 1-4, doi: 10.1109/IEDM50572.2025.11353866.

[3] S. Liao et al., "First Demonstration of CFET Ring Oscillator and SRAM Bit-Cell Functionality at Gate Pitch Smaller Than 48 nm for Future Logic," 2025 IEDM, pp. 1-4, doi: 10.1109/IEDM50572.2025.11353820.

[4] D. Ha et al., "3D Stacked FET (3DSFET) Logic and SRAM Technology Featuring Single Diffusion Break (SDB) and Back Side Interconnect (BSI) at 48 nm CPP for Advanced Mobile and High Performance Computing (HPC) Applications," 2025 VLSI, pp. 1-3, doi: 10.23919/VLSITechnologyandCir65189.2025.11074874.

[5] A. Dutta, G. Eneman, N. K. Thomas, P. Matagne and M. Radosavljević, "Stress in Single- and Multiribbon Complementary FETs (CFETs): Evolution in Process Flow and Impact on Drive Current," in IEEE Transactions on Electron Devices, vol. 72, no. 9, pp. 4735-4741, Sept. 2025, doi: 10.1109/TED.2025.3584743.